AMENDMENTS TO THE SPECIFICATION:

Please replace the Abstract with the following amended Abstract:

ABSTRACT OF THE DISCLOSURE

[1056] Operations including inserted prefetch operations that correspond to addressing chains may be scheduled above memory access operations that are likely-to-miss, thereby exploiting latency of the "martyred" likely-to-miss operations and improving execution performance of resulting code. More generally, certain pre-executable counterparts of likely-to-stall operations that form dependency chains may be scheduled above operations that are themselves likely-to-stall. ~~Techniques have been developed to perform such scheduling. In particular, techniques have been developed that allow scheduled pre-executable operations (including prefetch operations and speculative loads) to be hoisted above intervening speculation boundaries. Speculative copies of dependency chains are employed in some realizations. Aggressive insertion of prefetch operations (including some used as markers) is employed in some realizations. Techniques for scheduling operations (e.g., in a compiler implementation) are described. In various realizations, the techniques may be employed to select certain address chains to prefetch, to hide prefetch latency for the address chain prefetching code, and/or to transform code.~~